A Low Power VLSI Implementation of the Izhikevich Neuron Model

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***Abstract*— We present a low-power VLSI implementation of the Izhikevich neuron model utilizing two first-order log-domain filters as the main building block. One of the filters includes an active diode connection in order to lower current levels to obtain a low-power, large time constant design. Thus, the neuron circuit operates in sub-threshold regime with biological time scale. The possible applications of the presented implementation are simulating large scale VLSI neural networks and building hybrid interface systems. The simulation results demonstrate the success of replicating the firing patterns of real neurons.**

I. INTRODUCTION

There has been a growing interest in the last decade to realize VLSI implementations of biological neurons relying on the mathematical models, which vary in complexity and accuracy from the simple Integrate and Fire (I&F) model to the complex Hodgkin-Huxley (HH) model [1-10]. A possible application area of these implementations is designing neuromorphic systems including thousands of neurons coupled with each other on a single silicon wafer [11-16]. The aim of such systems is to observe neurocomputational properties of real neural systems and it is hoped to design silicon brains in the future. The challenge in designing such systems is to obtain a low power compact VLSI neuron circuit which can exhibit rich dynamics of the biological neurons. For this purpose, the choice of the I&F model, which is easy to implement electronically, would be inappropriate because of its poor dynamics, while the choice of HH model would lead to very complicated electronic circuit, despite offering rich dynamical behavior.

New low power and compact neuron designs operating at biological timescale have been proposed recently in [17, 18]. However, in these works, either the spike shapes are poor as in [17] or restricted dynamical behavior is obtained as in [18]. Nevertheless, there exists quite a popular model introduced by Izhikevich [19] which is not only computationally efficient providing easier electronic design but also can produce rich dynamical behavior. An excellent review of this model can be found in [20]. There are two simultaneous log-domain VLSI implementations of Izhikevich model [21, 22]. However, the circuit in [21] consumes much power and occupies much chip area for a large scale network design. Similarly, in [22], the circuit consumes considerable power for a 90nm design and the spike shapes are not fair considering different phases of an action potential such as depolarization and repolarization phases. In this work, we show that it is possible to realize power and area efficient log-domain Izhikevich VLSI neuron, while the circuit also mimics the dynamical behavior of the real neurons successfully. In section II, the mathematical model will be introduced and in section III, the circuit implementation will be presented. Simulation results will be given in section IV and the paper concludes with section V.

II. THE IZHIKEVICH MODEL

The Izhikevich model is first introduced in [19] and a detailed phase plane analysis with different set of parameters can be found in [20]. The main form of Izhikevich model is as given below:

$$\dot{v} = k(v - v_r)(v - v_t) - u + I_{in} \quad (1)$$

$$\dot{u} = a\{b(v - v_r) - u\} \quad (2)$$

$$if\ v \geq v_{peak}, v \leftarrow c, u \leftarrow u + d \quad (3)$$

where v is the membrane potential, u is the recovery current, v_r is the resting membrane potential, v_t is the instantaneous threshold potential, I_{in} is the external input current, k is a scaling coefficient, v_{peak} is the spike cutoff value, c is the reset value of variable v and d is the increment amount of variable u at reset time. A possible selection of parameters that leads to typical neuron behavior may be, k = 1.5, v_r = -60, v_t = -40, a = 1, b = 4, v_{peak} = 35, c = -50 and d = 100. For these parameter values, regular spiking is observed with an approximate period of 1.8 s where v takes value between (-60,+35) and u changes between (60,160). It should be noted that the parameters k, a and b are dimensionless and the rest of parameters has the same dimension with two variables.

For a proper log-domain implementation of the model equations in (1-3), the state variables should be given in terms of currents with positive values. Hence, model equations are altered in order to shift the equilibrium point such that the instantaneous values of variables u and v become always positive. For this purpose, the variable v is shifted up by an amount of v_{offset} while the variable u is shifted up by $b(v_{offset} + v_r)$. Additionally, for low-power operation, the magnitudes of the variables are scaled such that the currents are in the pA range. After proper shifting and magnitude scaling, the new set of equation is obtained as follows:

$$\tau \dot{I}_v = kI_v(I_v - I_a)10^{12} + (I_{DC} + I_{in} - I_u) \quad (4)$$

$$\tau \dot{I}_u = a(bI_v - I_u) \quad (5)$$

$$if\ I_v \geq I_{peak}, I_v \leftarrow I_c, I_u \leftarrow I_u + I_{incr} \quad (6)$$

where I_{DC} stands for the current required for DC level shifting of variables I_v and I_u, I_a is the shifted threshold value, I_{peak} is the spike cutoff value, I_c is the reset value of I_v and finally I_{incr} is the amount of increment of I_u at reset time. Note that all the terms, except the time constant τ and dimensionless parameters k, a and b, are currents in the pA range.

III. Circuit Implementation

As the main building block of the neuron circuit realizing the model equations in (4-6), we consider the first-order log-domain filter in Fig. 1. In this circuit, all the transistors operate in subthreshold region with an *i-v* relationship given by:

$$I_{DS} = I_s \frac{W}{L} \exp(\alpha V_{GS}) \quad (7)$$

where α is a parameter with an approximate value of 33. Using translinear principle, one can easily show that the state equation of this circuit is,

$$C\dot{I}_{out} = -I_{out}(\alpha I_d) + I_{in}(\alpha I_b)(r_2 r_4 / r_1 r_3) \quad (8)$$

where r_1-r_4 are the aspect ratios of M_1-M_4 respectively. In order to obtain an expression similar to that in (8), we rearranged (4-5) and obtained the following system equations to be used to realize the final neuron circuit.

$$C_v \dot{I}_v = -I_v(I_a - I_v)10^{12} kC_v/\tau + (I_{DC} + I_{in} - I_u)C_v/\tau \quad (9)$$

$$C_u \dot{I}_u = -I_u(aC_u/\tau) + I_v(abC_u/\tau) \quad (10)$$

These two state equations can readily be realized using a pair of the log-domain filter structure in Fig. 1. The circuit thus obtained with additional circuitry for reset dynamics is shown in Fig. 2. The values of the parameters are chosen as k =1.5, a = 1, and b = 4. For a low area design, the values of the capacitors are set to C_u = C_v = 500fF, the time constant is chosen $\tau \cong 25$. Thus, the values of the DC currents are $I_{d\text{-}u}$ = 250fA, $I_{b\text{-}u}$ = 1pA, $I_{d\text{-}v}$ = 7.5pA and $I_{b\text{-}v}$ = 250fA, I_{DC} = 90pA. With these values, the peak value of variable I_v become I_{peak} = 90pA. The transistors M_5-M_8 realize the differential equation in (10) related to I_u, while M_{11}-M_{14} and M_{16} realize the state equation in (9) related to I_v. The transistors M_{10} and M_{15} serve as a switch to reset the current I_v to I_c and I_u to I_u+I_{incr}. The values of the currents I_c and I_{inc} are made adjustable through the voltages V_c via M_{15} and V_d via M_9, respectively. Transistors M_{17}-M_{19} compose multiple output current mirror generating replicas of the current I_v, and the comparator along with the NOT gates produce the voltages V_{reset} and $\overline{V_{reset}}$. The diode connection of M_{13} is supplied by a buffer which is indeed a simple differential pair with a 35pA bias current.

The crucial point of this design is the shifted source voltages and the active diode connection which enables transistors to handle low current levels at a few ten of hertz frequency, resulting in a circuit with very low power consumption.

To be clear, a usual way of comparison done for current-mode

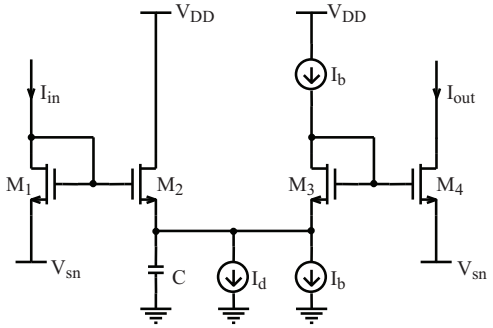

Figure 1. Log domain integrator.

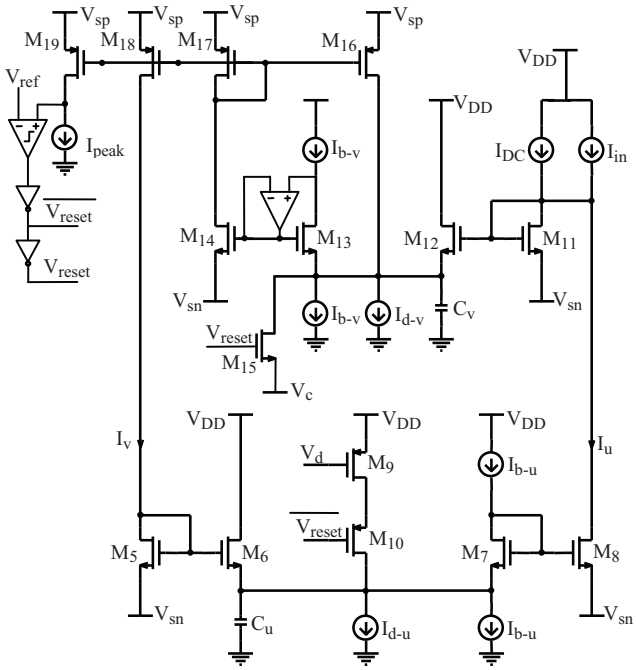

Figure 2. The proposed neuron circuit.

circuits [23, 24] is made between classical (CM), source shifted (SSCM) and active diode connected (ACM) current mirrors that are shown in Fig. 3. DC worst case analysis results of the current mirrors are shown in Fig. 4. The x axis is input current swept from 1fA to 100pA and y axis is the output current. It is obvious that source shifting definitely improves DC behavior and active diode connection also makes an improvement. Note from Fig. 2 that all the transistors have shifted sources and all the currents are above 1pA except $I_{b\text{-}v}$ = 250fA. It is seen from Fig. 4 that standard

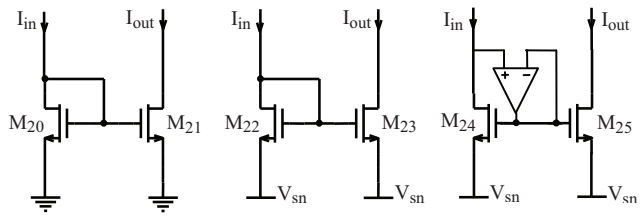

Figure 3. Current mirror toplogies (a) classical; (b) source shifted and (c) active diode connected.

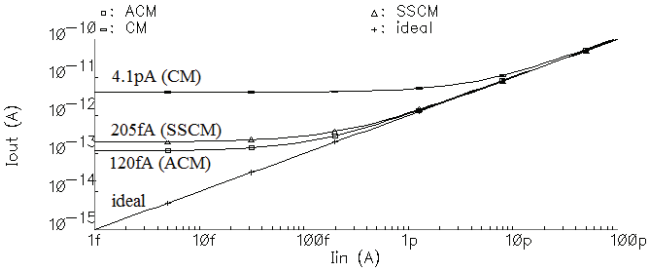

Figure 4. DC response of CM, SSCM and ACM.

CM topology is not an option in our design because of its poor DC performance at current levels below 1pA. Therefore, either SSCM or ACM should be used to obtain proper DC behavior. On the other hand, AC worst case analysis results are given in Fig. 5. Since CM topology is eliminated due to its very large DC gain error, we have only compared SSCM and ACM topologies. The AC bandwidth improvement of ACM with respect to SSCM, while the DC input current is 250fA, can be clearly seen from the simulation results given in Fig. 5. From Fig. 4 and 5, it can be concluded that source shifting is an appropriate solution for a minimum level of 1pA current for an acceptable AC and DC behavior, where only $I_{b\text{-}v}$ is an exception of this condition in Fig. 2. Active diode connection is also enough for a minimum level of 250fA current for proper AC and DC behavior. Therefore, transistor M13 in Fig. 2 has such a connection in order to supply this very low $I_{b\text{-}v}$ current. In fact, an alternative topology exist in [23, 24] utilizing a high-gain opamp. However, this topology is inconvenient for our design because of the high biasing currents of the opamp resulting in high power consumption.

IV. Simulation Results

The circuit in Fig. 2 is simulated using AMS 0.35µm process parameters using Spectre in Cadence design tool. Supply voltage is V_{DD} = 1.65V and source shifting amount is 400mV. Reference voltage of the comparator is set to $V_{ref} = V_{DD}/2$. All the transistors have W/L=1µ/1µ except for M_{16}, the positive feedback transistor, with a ratio W/L = 1µ/2.5µ. The tuning range of V_c and V_d are (480,505) mV and (350,500) mV respectively. It should be noted that, in (8), I_b and the aspect ratios of transistors composing the translinear loop appear as a product term for the log-domain filter block. Therefore, the deviations of transistors' aspect ratios can be tolerated by adjusting $I_{b\text{-}v}$ and $I_{b\text{-}u}$ currents in Fig. 2.

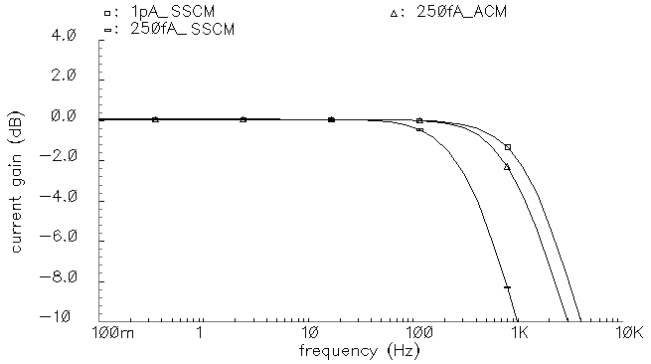

Figure 5. AC response of SSCM and ACM

The estimated chip area is 1100µm^2. At resting state, i.e. zero input state, I_v = 3.3pA, I_u = 14.3pA and the current and power consumption of the circuit is 147.2pA and 243pW, respectively. While the circuit is in regular spiking regime with a period of 100ms, the circuit consumes 1.65nW. This is

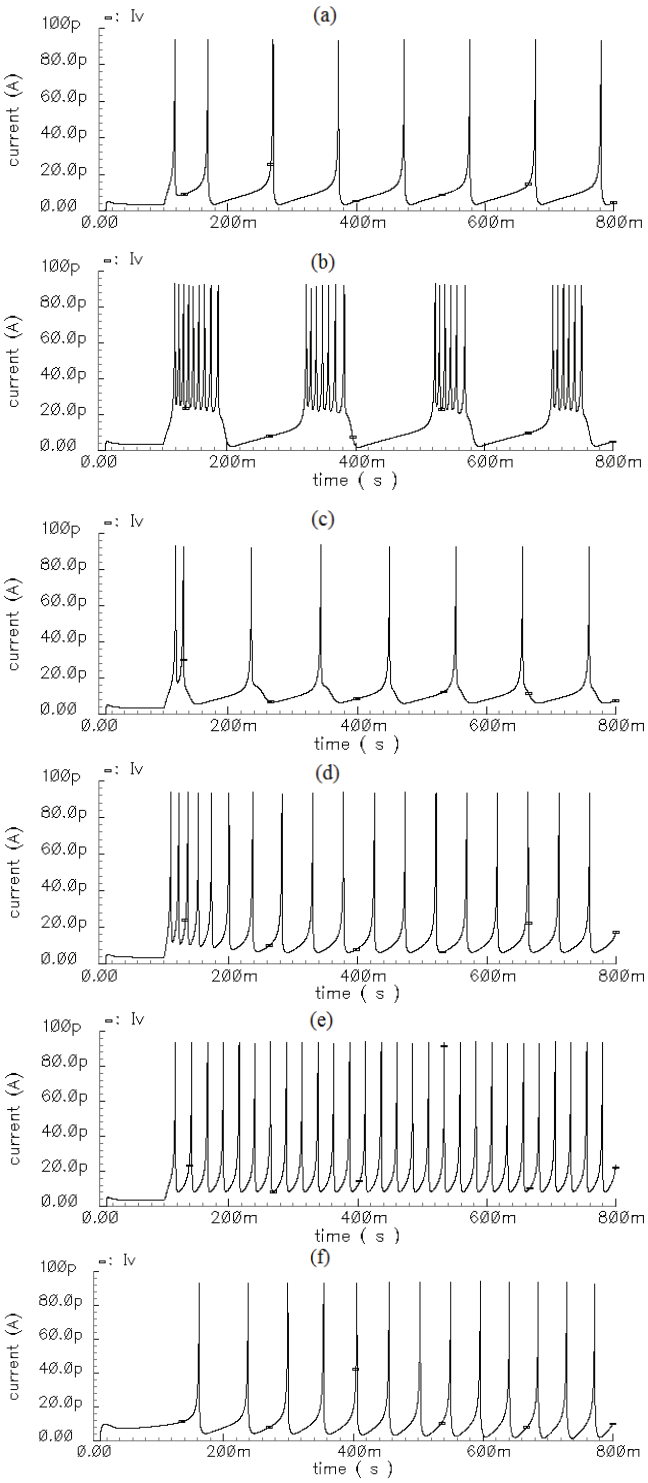

Figure 6. Firing patters. (a) Regular Spiking; (b) Bursting; (c) Intrinsically bursting; (d) Low Threshold Spiking (Spike Frequency Adaption); (e) Fast Spiking; (f) Class II Behavior

a very low value when compared to results in [21] and [22]. Additionally, Monte Carlo simulations are done and the circuit still exhibits successful spiking behavior.

Fig. 6 shows different type of firing patterns reproduced from the circuit. The input is a step current except in Fig. 6f where it is a ramp current. Only V_c and V_d are tuned in the circuit to observe Fig. 6a-d and $I_{b\text{-}u}$ and $I_{d\text{-}u}$ are additionally tuned for Fig. 6e. Since $b > 0$ in this design, the neuron circuit behaves as a resonator rather than an integrator. Therefore, we expect to see a *Class II* behavior as depicted in Fig 6f. Here, the neuron starts to fire at a non-zero frequency while excited with a ramp input current.

At this point, we want to note a general mistake done in the literature while interpreting the dynamical properties of firing patterns in *Class II* resonator. In *Class II* behavior, observing long periodic behaviors by supplying very low input currents or resetting the first variable to a low value may mislead to conclude the neuron as an integrator, i.e. shows *Class I* behavior. However, in order to properly justify the *Class* of the behavior, the firing patterns should be studied and obtained following the way explained in [20] by exciting the neuron by a ramp input current and obtaining *f-I* characteristic of the neuron. The study of the dynamical behavior of the proposed neuron model according to this approach leads us to conclude that the proposed circuit is indeed a *Class II* neuron.

The similarity between the firing patterns observed in this work and the numerical results in [19, 20] shows the success of the design.

V. CONCLUSION

We have implemented Izhikevich neuron model in log-domain and with the aid of additional active diode connection, we have obtained a low power compact VLSI circuit and observed typical firing patterns of a neuron successfully.

Low power and compact design makes the circuit suitable for building human interface electronics systems or large scale neuromorphic systems to simulate complex neural systems such as human brain.

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